Evolvable Hardware for Space Applications

Authors:	Jason Lohn, James Crawford, Al Globus, Gregory Hornby, William Kraus, Gregory Larchev, Anna Pryor
Affiliation:	NASA Ames Research Center
Address:	MS 269-1, NASA Ames Research Center, Moffett Field, CA 94035
Email:	Jason.D.Lohn@nasa.gov
Phone:	650-604-5138

Abstract:

The Evolvable Systems Group at NASA Ames Research Center has developed the ability to use evolutionary algorithms (EAs) for spacecraft antenna design, fault tolerance for programmable logic chips, analog [Lohn and Colombano 1998] and digital [Lohn et al. 2002] circuit design. In some of these areas, evolutionary algorithms match or improve on human performance. Due to space limitations for this abstract, we discuss selected areas:

Spacecraft Antenna Design

Designing antennas by hand is slow and requires great expertise. We have automated antenna design using a tree-structured representation which matches the tree-structure of the corresponding antennas. We have evolved small, efficient antennas for NASA's Space Technology 5 mission that, according to simulation, meet the requirements. In addition, the fitness function evaluates an antenna design multiple times, each with a small random perturbation applied to joint angles and wire radii to account for manufacturing tolerances. The addition of manufacturing noise results in antennas that perform well across a broad range of frequencies.

Self-repairing FPGAs

Space radiation is significant threat to spacecraft avionics. Shielding and redundancy play an important role in radiation mitigation, but new techniques are proving to show promise. We have demonstrated that field-programmable gate array chips can be rapidly reconfigured under evolutionary search in order to repair permanent latch-up fault damage. Because FPGAs can be rapidly reconfigured at hardware speeds, this approach shows promise in being able to provide fault-recovery at real-time or near real-time speeds.

References

[J. Lohn, G. Larchev and R. DeMara] A Genetic Representation for Evolutionary Fault Recovery in Virtex FPGAs, The 5th International Conference on Evolvable Systems (ICES 2003), Trondheim, Norway, March 2003.

[Lohn and Colombano 1998] Jason D. Lohn and Silvano P. Colombano, "Automated Analog Circuit Synthesis Using a Linear Representation," Second International Conference on Evolvable Systems: From Biology to Hardware, Springer-Verlag, 23-25 September 1998.

[Lohn et al. 2002] J.D. Lohn, G. Larchev, R. DeMara, "A Genetic Representation for Evolutionary Fault Recovery in FPGAs," International Conf. on Military and Aerospace Programmable Logic Devices, Laurel, MD, September 10-12, 2002.